IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes et al.	Examiner: Son Dinh
Serial No.:	09/945,507	Group Art Unit: 2824
Filed:	August 30, 2001	Docket: 1303.014US1
Title:	FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS	

COMMUNICATION CONCERNING RELATED APPLICATION(S)

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicants would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

Serial/Patent No.	Filing Date	Attorney Docket	Title
10/931704	September 1, 2004	1303.014US2	FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/929986	August 30, 2004	1303.045US2	ATOMIC LAYER DEPOSITION OF METAL OXIDE AND/OR LOW ASYMMETRICAL TUNNEL BARRIER INTERPOLY INSULATORS
10/931711	September 1, 2004	1303.029US2	PROGRAMMABLE MEMORY ADDRESS AND DECODE CIRCUITS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/931540	August 31, 2004	1303.020US2	PROGRAMMABLE ARRAY LOGIC OR MEMORY DEVICES WITH ASYMMETRICAL TUNNEL BARRIERS
	February 10, 2005	1303.130US1	ATOMIC LAYER DEPOSITION OF CeO2/Al2O3 FILMS AS GATE DIELECTRICS
	February 8, 2005	1303.131US1	ATOMIC LAYER DEPOSITION OF DY-DOPED HFO2 FILMS AS GATE DIELECTRICS

Respectfully submitted,

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By Applicants' Representatives,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 15 day of February, 2005.

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